Multi-phase Boiling Analysis for Liquid Cooled Expanding Micro-channels

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The recent development of high power micro-electronic chip stacking technology has provided a possible path for increasing performance for high speed computing. However, the heat load generated by the 3D chip stacks poses a significant challenge in thermal management for large arrays. Traditional cooling methods using air and internal fans are not able to provide sufficient cooling required to maintain the stack temperature within normal operation range. A highly feasible solution is to use "liquid cooling" to replace air cooled systems for several reasons: air is a poor conductor of heat compared to liquid, and liquid has a higher heat capacity than air allowing it to remove heat from the stacks more effectively.

The idea of using liquid cooling for micro-channels has been proposed recently. However, in practice, this method requires a closed system to circulate liquid within the system. Many high power systems today generate an excessive amount of heat, causing the cooling liquid to quickly reach its boiling temperature and convert into vapor bubbles. As the heating continues, more and more vapor will be generated to form pockets of vapor, eventually becoming an annular mist region downstream of the channel. In addition, the excessive heating may create local dried out spots in the micro-channel passage, leading to overheating and damage to the micro-channel. Although the use of liquid cooling provides a potentially efficient method, better system technology development, closed liquid system management, and the understanding of multi-phase liquid boiling phenomena are required to achieve practical implementation.

The present work proposes a two-phase cooling approach, utilizing a chip-to-chip interconnect-compatible dielectric fluid. The cooling is achieved by flowing dielectric coolant through channels fabricated within the silicon chip, where the fluid is converted from liquid phase to gaseous phase as it flows. This chip-integrated micrometer-scale two-phase cooling technology can be essential to fully optimize the benefits of improved integration density and modularity of 3D stacking of high performance integrated circuits (ICs) for future computing systems. The fundamental challenge is to integrate variations in coolant saturation temperature, local heat transfer and friction coefficients, and vapor quality with the complex conduction problem involving the microprocessor package.

An Eulerian multiphase model has been developed for simulating two-phase evaporative cooling through chip embedded microscale cavities. Complex flow geometries are expected in microprocessor chip-stacks with chip-to-chip interconnects. A representative geometry is shown in Figure 1. The fluidic channels are formed by bonding two silicon chips into a "die pair" to achieve channels of roughly 120μm height. The flow path, as illustrated in Figure 1, includes a central inlet manifold and radial channels to direct the flow of a dielectric fluid from the center of a chip to its periphery. The inlet orifices, also shown in Figure 1, were designed to have a width appropriate to the expected power to be dissipated by the coolant flowing in each radial segment. As the dielectric fluid absorbs heat and evaporates within the micro scale cavities, the resulting two phase flow moves radially outward through a network of hierarchical radial channels to the outlet plenum, where it is collected.

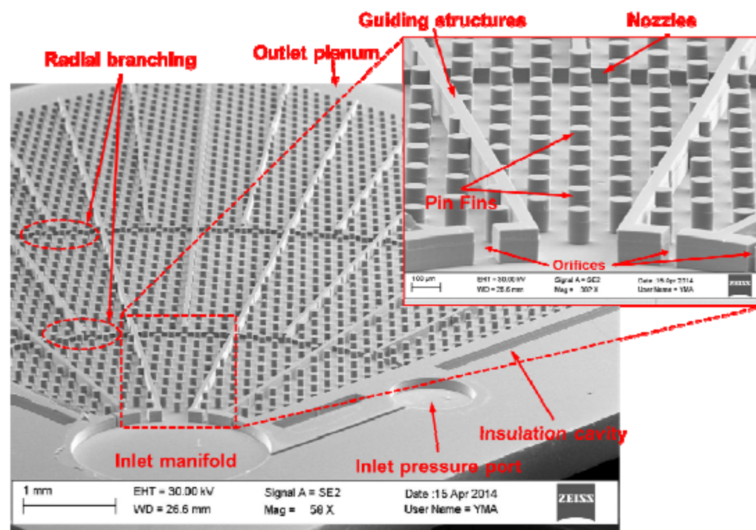


Figure 1. Radial channel structure with pins representing chip-to-chip interconnection.

For the multi-phase expanding channel boiling analysis, if we include the entire channel with all the pins, the computational mesh required to resolve the heat transfer and two-phase boiling next to each pin's surface can be prohibitive. To make the two-phase boiling analysis more computational economic, only a representative sub-domain as shown in Figure 2(a), is modeled. It represents a section with an 18 degree divergence angle, with fluid cavity height og 120 µm, and the pin-field consisting of 80 µm diameter pins arranged in a 200 µm pitch square grid. The silicon chip thickness is considered to be 50 µm. In this model, both the top and the bottom silicon are active with dissipated heat fluxes of 50 W/cm2 each. A high pressure dielectric coolant (R1234ze) is considered as the coolant. A nominal flow rate of 0.1 g/s with saturation conditions of 30 C is assumed at the channel inlet. Figure 2(b) shows the computational mesh. The mesh has about 1.5 million elements total with 1.12 million elements in the fluid domain and 0.34 million elements in the solid domains including the pins and top and bottom silicon plates.

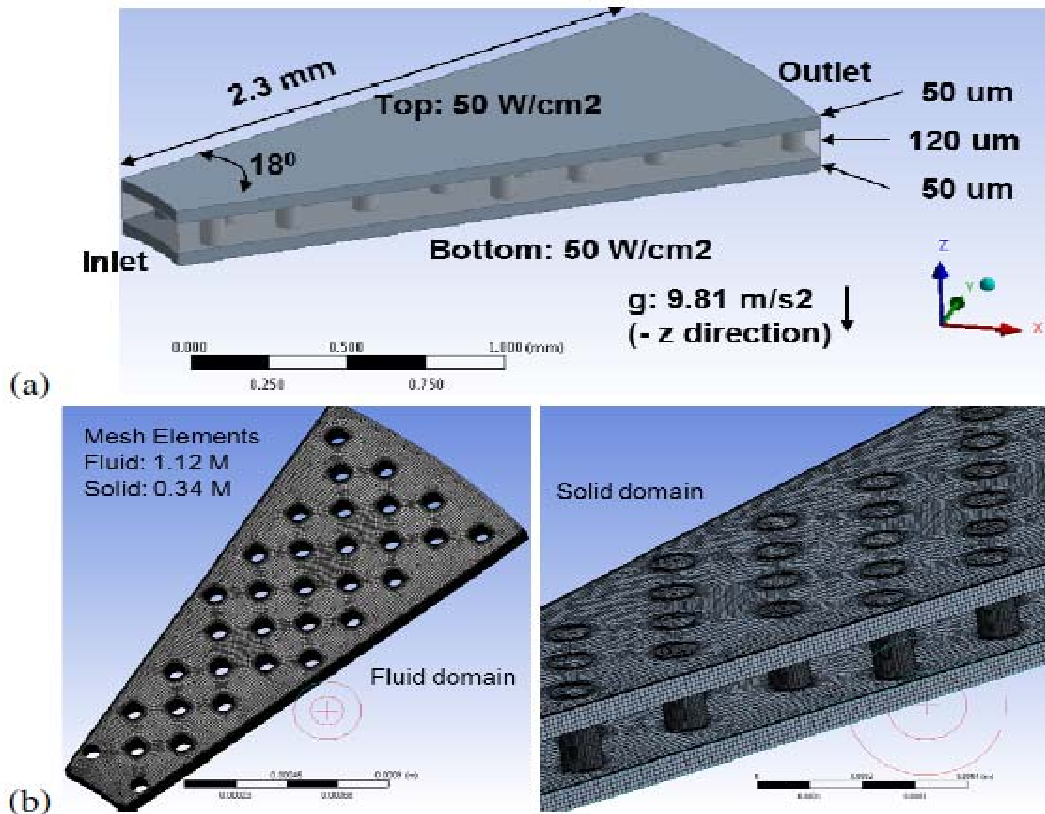


Figure 2(a) Representative section of the expanding channel, (b) computation mesh

To perform the multi-phase boiling analysis, the Eulerian multiphase model with wall boiling and critical heat flux in ANSYS Fluent is used. This model treats each phase (liquid and vapor) as interpenetrating continua and uses the concept of phasic volume fraction to keep track of different phases in a given computational cell. In this model, a common pressure field is shared by all the phases. The model has increased complexity as it solves a set of continuity, momentum and energy equations for each phase. Coupling between liquid and vapor phases is captured through the common pressure field and through momentum and energy exchange sub-models such as interphase drag, lift, continuum surface force, heat and mass transfer models across the fluid-solid interface, etc. In addition, a k-ε mixture turbulence model is used to capture the turbulent interaction between the liquid and vapor phase. In this mixture model one set of k-ε equations is solved for all phases present. Further, at the fluid-solid interfaces/walls, wall heat flux partitioning models are used. Table 1 and 2 summarize the material properties and boundary conditions used for the two-phase simulation.

Coolant:	R1234ze (Mol. wt.: 114.0416 kg/kmol)
Liquid phase:	$\rho_l = 1146.3 \, kg/m^3$ $C_{pl} = 1401.2 \, J/kg-K$ $\mu_l = 0.000188 Pa-s$ $\lambda_l = 0.072675 \, W/m-K$
Vapor phase:	$\rho_v = 30.564 \, kg/m^3$ $C_{pv} = 1007.1 \, J/kg-K$ $\mu_v = 12.458e-6 Pa-s$ $\lambda_v = 0.014056 \, W/m-K$
Latent Heat:	$H_{lv} = 162900 \, J/kg$
Surface Tension:	$\sigma = 0.00821 \, N/m$
Saturation Temperature:	
$T_{sat}(p_{abs})[C] = -0.3845 * \left(\frac{p_{abs}}{1[bar]} \right)^2 + 10.392 * \left(\frac{p_{abs}}{1[bar]} \right) - 17.246[C]$	

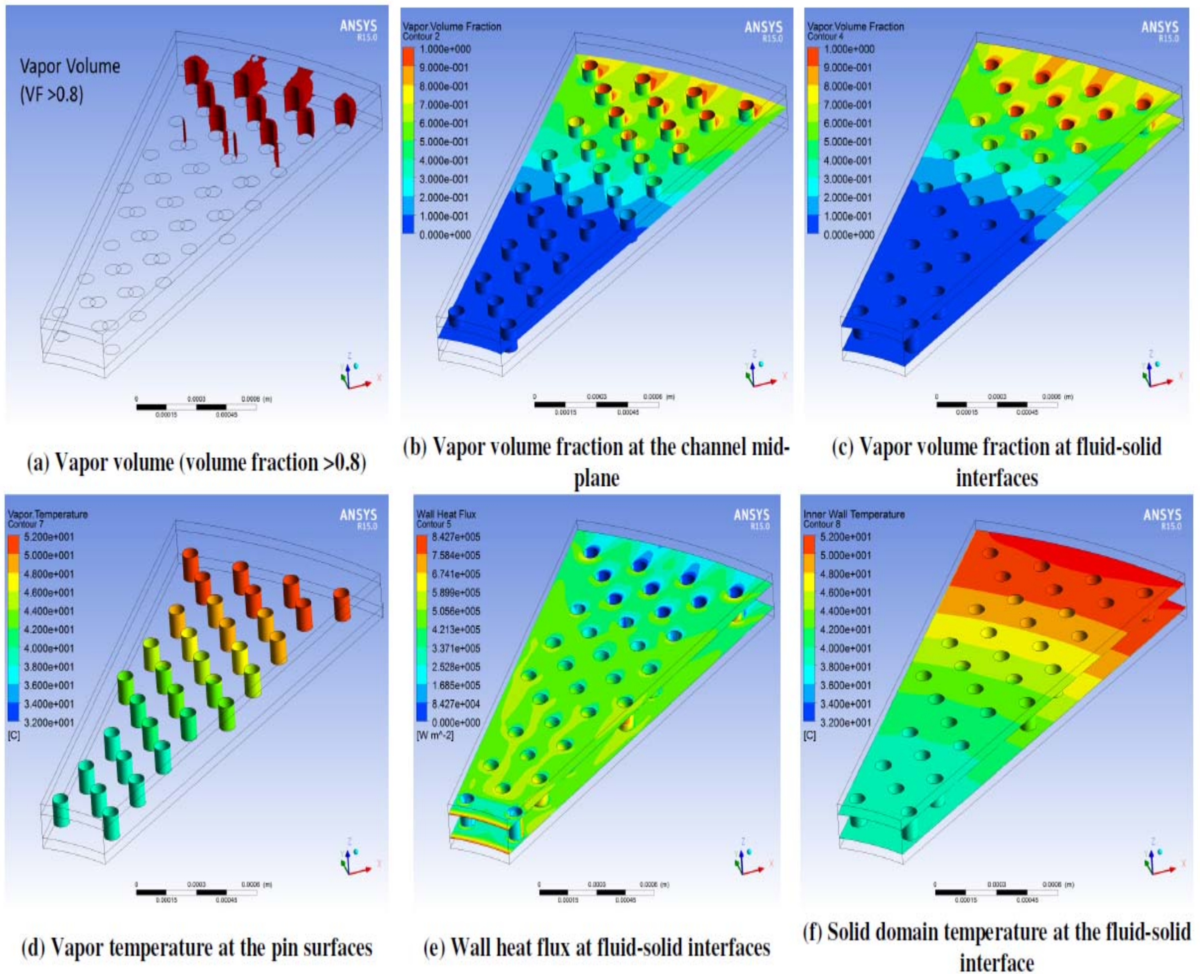
Table 1. Coolant material properties

Fluid domain	R1234ze
Inlet	0.1 g/s, 30 [ºC]
Ref. Pressure	578.43 kPa
Outlet	0 relative pressure
Walls	Wall heat flux partitioning, No-slip.
Solid domain	Silicon
Top & Bottom Surface	50 W/cm^2

Table 2. Boundary conditions for the expanding channel analysis

Figure 3 shows the detailed simulation predictions for the vapor volume fraction, vapor temperature, wall heat fluxes and active surface temperature. The pressure drop across the channel was predicted to be ~17 kPa. The average outlet vapor quality is predicted to be 6.6% with average volume fraction of 72.6%. Figure 3(a) shows the vapor volumes. The model predicts the vapor to form initially at the rear portion of the downstream pins, suggesting that the pins act as bubble nucleation sites. Moreover, the low pressure zone created at the trailing edge of the pins facilitates the formation of bubbles. Figures 3(b) and 3(c) show the vapor volume fraction prediction at the channel mid-plane and at the fluid-solid interfaces, respectively. It can be seen that for the flow rate and coolant inlet temperatures considered, the vapor starts to form around the middle of the channel and expands quickly to occupy most of the channel cross-section near the channel outlet. Figure 3(d) shows the vapor temperature contours at the pin surfaces. Since the pressure gradient is not as steep as that observed for straight channels, and also because the flow velocities reduce along the channel, the vapor temperature increases steadily from inlet to outlet. Figure 3(e) shows the wall heat flux contours at the fluid-solid interfaces. The wall heat flux at the fluid-solid interfaces shows a non-uniform distribution, with most of the heat flowing into the coolant in the initial section of the channel. This suggests that the convective heat transfer term is dominating the wall heat flux partition. Figure 3(f) shows the prediction for solid domain temperature at the fluid-solid interface. Similar to the vapor temperature, the solid temperature is observed to be increasing from inlet to outlet. Part of this behavior can be attributed to the fact that this is a low vapor

quality flow, where the single phase convective heat transfer component is dominant and that for diverging flows, the convective heat transfer rate reduces as the flow velocity reduces.



(a) Vapor volume (volume fraction >0.8)
(b) Vapor volume fraction at the channel mid-plane
(c) Vapor volume fraction at fluid-solid interfaces
(d) Vapor temperature at the pin surfaces
(e) Wall heat flux at fluid-solid interfaces
(f) Solid domain temperature at the fluid-solid interface

Figure 3. Detail simulation results for vapor volume, vapor volume fraction, vapor temperature, wall heat flux and solid temperature for the expanding channel with pins